

## CLAIMS

I claim:

1. A system comprising:

a plurality of functional blocks, and

a bus structure that is configured to facilitate communications among the plurality of functional blocks,

wherein

at least one functional block of the plurality of functional blocks includes

a bus interface adapter that is configured to provide either of two modes of operation, such that communications via the bus structure are synchronous in a first mode of operation, and asynchronous in a second mode of operation.

2. The system of claim 1, wherein

the bus interface adapter includes at least one delay device for delaying control signals that are communicated via the bus, and

the at least one delay device is configured to be bypassed during the first mode of operation, and used for delaying control signals during the second mode of operation.

3. The system of claim 1, wherein

the at least one functional block is embodied in an integrated circuit that includes a plurality of conductive layers, and

the bus interface adapter is configured to provide either the first or the second mode of operation based on a configuration of interconnections at an upper layer of the plurality of conductive layers.

4. The system of claim 1, further including

a bus controller that is configured to control the communications among the plurality of functional blocks, and includes a plurality of bus interface modules,

at least one bus interface module of the plurality of bus interface modules being configured to selectively provide either synchronous communications or asynchronous communications via the bus structure.

5. The system of claim 4, wherein

the bus controller includes one or more delay devices that are configured to delay control signals that are communicated among the plurality of functional blocks, thereby facilitating communication of data between a first functional block and a second functional block of the plurality of functional blocks using an asynchronous communication with the first functional block and a synchronous communication with the second functional block.

6. The system of claim 4, wherein

the bus controller is embodied in an integrated circuit that includes a plurality of conductive layers, and

the at least one bus interface module is configured to selectively provide either the synchronous or the asynchronous communications based on a configuration of interconnections at an upper layer of the plurality of conductive layers.

7. The system of claim 4, wherein

the bus controller is further configured to:

determine if communications with the at least one functional block can be effected via synchronous communications, and

cause the bus interface adapter to enter the second mode of operation only if communications with the at least one functional block cannot be effected via synchronous communications.

8. A bus controller comprising

a plurality of bus interface modules that facilitate communications among a plurality of functional blocks via a communications bus,

wherein

at least one bus interface module of the plurality of bus interface modules is configured to selectively provide either synchronous or asynchronous communications via the communications bus.

9. The bus controller of claim 8, further including

at least one delay device that is configured to delay control signals that are communicated among the plurality of functional blocks via the communications bus, when the at least one bus interface module is configured to provide asynchronous communications.

10. The bus controller of claim 8, wherein

the bus controller facilitates communication of data between a first functional block and a second functional block of the plurality of functional blocks via asynchronous communication with the first functional block and synchronous communication with the second functional block.

11. The bus controller of claim 8, wherein

the bus controller is embodied in an integrated circuit having a plurality of conductive layers, and

the at least one bus interface module is configured to selectively provide either synchronous or asynchronous via a configuration of interconnections at an upper layer of the plurality of conductive layers.

12. The bus controller of claim 8, wherein

the bus controller is configured to:

determine if communications with at least one functional block of the plurality of function blocks can be effected via synchronous communications, and

selectively provide asynchronous communications to the at least one functional block if communications with the at least one functional block cannot be effected via synchronous communications.

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13. A method of facilitating communications in a system that comprises a plurality of functional blocks that communicate via a bus structure, comprising:

creating a layout of the plurality of functional blocks,

determining a clock skew associated with at least one functional block of the plurality of functional blocks, based on the layout, and

selectively configuring the at least one functional block for either asynchronous or synchronous communications via the bus structure, based on the clock skew.

14. The method of claim 13, wherein

the system is embodied in an integrated circuit having a plurality of layers, and

selectively configuring the at least one functional block includes determining a configuration of interconnections at an upper layer of the plurality of layers to provide either asynchronous or synchronous communications with the bus structure.

15. The method of claim 13, wherein

selectively configuring the at least one functional block includes configuring the at least one functional block to provide a delay to control signals that are communicated between the at least one functional block and the bus structure.

16. The method of claim 13, wherein

the system includes a bus controller, and

selectively configuring the at least one functional block includes configuring the bus controller to provide a delay to control signals that are communicated between the bus controller and the bus structure.